AMENDMENTS TO CLAIMS

Claims 1 - 66 (cancelled)

Claim 67 (currently amended): Circuitry for protection of an integrated circuit, which integrated circuit includes operational-circuits formed on a chip, the circuitry comprising:

a plurality of detectors, integrally formed on the chip as part of the integrated circuit and dispersed among the operational-circuits on the chip, the detectors being adapted, in response to radiation incident on the chip, to trigger a security measure so as to prevent tampering with the integrated circuit,

wherein the operational-circuits include components having predefined attributes, and wherein the detectors are formed by modifying at least one of the attributes of one or more of the components so as to alter the response of the detectors to the radiation relative to the response of the components having the predefined attributes, and

wherein the predefined attributes are chosen from at least one of layout attributes, layout dimensions, manufacturing-process attributes, doping dosage, adding a sub-element of the component, removing the sub-element of the component, and materials type.

Claim 68 (cancelled)

Claim 69 (previously presented): The circuitry according to claim 67, wherein at least one of the detectors comprises a p-channel transistor coupled in series with an n-channel transistor, and wherein in response to the radiation a conductance of the p-channel transistor is substantially different from the conductance of the n-channel transistor.

Claim 70 (previously presented): The circuitry according to claim 67, wherein at least one of the detectors comprises a memory, and wherein the security measure comprises a change of state of the memory.

Claim 71 (previously presented): The circuitry according to claim 67, wherein the integrated circuit is implemented according to a technology chosen from at least one of metal oxide semiconductor and bipolar technologies.

Claim 72 (previously presented): The circuitry according to claim 67, wherein the chip is a semiconductor chip.

Claim 73 (previously presented): The circuitry according to claim 67, wherein the radiation comprises at least one type of radiation chosen from electromagnetic radiation and ionizing radiation.

Claim 74 (previously presented): The circuitry according to claim 67, wherein the plurality of detectors are chosen from at least one biased-low detector which is operative to generate a logic low level in response to the radiation and at least one biased-high detector which is operative to generate a logic high level in response to the radiation.

Claim 75 (previously presented): The circuitry according to claim 67, and comprising a roughened chip surface that defocuses the radiation.

Claim 76 (previously presented): The circuitry according to claim 67, wherein the tampering comprises a fault being inserted into one of the operational-circuits so as to cause a functional result in the integrated circuit.

Claim 77 (previously presented): The circuitry according to claim 67, wherein at least one of the detectors is coupled to serve as one of the components in one of the operational-circuits.

Claim 78 (previously presented): The circuitry according to claim 77, wherein the one of the operational-circuits functions according to predefined specifications while the radiation is not incident thereon.

Claim 79 (previously presented): The circuitry according to claim 78, wherein the one of the operational-circuits functions differently from the predefined specifications while the radiation is incident thereon.

Claim 80 (previously presented): The circuitry according to claim 67, wherein the components comprise transistors, and wherein the response of the detectors comprises an altered conductance of the transistors.

Claim 81 (previously presented): The circuitry according to claim 67, wherein the response of the detectors comprises a change in an operational level of the operational-circuits.

Claim 82 (previously presented): The circuitry according to claim 67, wherein the response of the detectors comprises a change in a signal timing of the operational-circuits.

Claim 83 (previously presented): The circuitry according to claim 67, wherein the radiation comprises detector-triggering radiation, and wherein a level of the detector-triggering radiation is less than the level of radiation that affects a functionality of the operational-circuits while being sufficient to trigger the detectors.

Claim 84 (previously presented): The circuitry according to claim 83, wherein the radiation comprises optical radiation.

Claim 85 (previously presented): The circuitry according to claim 67, and comprising an auxiliary circuit which is coupled to at least one of the plurality of detectors and which is implemented to receive a trigger signal from the at least one of the detectors.

Claim 86 (previously presented): The circuitry according to claim 85, wherein the

trigger signal is received as the security measure and wherein the auxiliary circuit is implemented to generate a control signal in response thereto, and comprising a control circuit which is coupled to receive the control signal so as to initiate an alarm in response thereto.

Claim 87 (previously presented): The circuitry according to claim 85, wherein the auxiliary circuit comprises elements selected from the operational-circuits and the detectors so as to provide an indication of the radiation in response to the radiation being incident on at least a part of the auxiliary circuit.

Claim 88 (previously presented): The circuitry according to claim 85, wherein the auxiliary circuit comprises a memory, and wherein the indication comprises a change of state of the memory.

Claim 89 (previously presented): The circuitry according to claim 85, wherein the auxiliary circuit has an asymmetric response to the radiation, and is implemented to convey an indication of the radiation to a signal receiver regardless of the radiation on the auxiliary circuit.

Claim 90 (previously presented): The circuitry according to claim 67, and comprising one or more auxiliary circuits coupled to at least one of the detectors and having an asymmetric response to the radiation.

Claim 91 (previously presented): The circuitry according to claim 90, wherein the one or more auxiliary circuits comprise a biased-low auxiliary circuit configured to output a logic low level in response to the radiation and a biased-high auxiliary circuit configured to output a logic high level in response to the radiation, and wherein the biased-low auxiliary circuit and the biased-high auxiliary circuit are connected in series.

Claim 92 (previously presented): The circuitry according to claim 67, wherein the plurality of detectors comprises a memory comprising at least one of a biased-low

detector which is operative to generate a logic low level in response to the radiation and a biased-high detector which is operative to generate a logic high level in response to the radiation.

Claim 93 (previously presented): The circuitry according to claim 92, wherein the biased-low detector and the biased-high detector are coupled in series.

Claim 94 (canceled)

Claim 95 (canceled)

Claim 96 (previously presented): A method for protection of an integrated circuit, which integrated circuit includes operational-circuits formed on a chip, the method comprising:

integrally forming a plurality of detectors on the chip as part of the integrated circuit, so that the detectors are dispersed among the operational-circuits on the chip, the detectors being adapted, in response to radiation incident on the chip, to trigger a security measure so as to prevent tampering with the integrated circuit, and also forming an auxiliary circuit which is coupled to at least one of the plurality of detectors,

wherein at least one of the following has an enhanced asymmetric response to the radiation: at least one of the plurality of detectors; and the auxiliary circuit.

Claim 97 (previously presented): Circuitry for protection of an integrated circuit, which integrated circuit includes operational-circuits formed on a chip, the circuitry comprising:

a plurality of detectors, integrally formed on the chip as part of the integrated circuit and dispersed among the operational-circuits on the chip, the detectors being adapted, in response to radiation incident on the chip, to trigger a security measure so as to prevent tampering with the integrated circuit, the chip comprising a roughened chip surface that defocuses the radiation.

Claim 98 (previously presented): The circuitry according to claim 97 and wherein the roughened chip surface comprises a lower surface.

Claim 99 (previously presented): The circuitry according to claim 97 and wherein the roughened chip surface comprises an upper surface.

Claim 100 (previously presented): A method for protection of an integrated circuit, which integrated circuit includes operational-circuits formed on a chip, the method comprising:

integrally forming a plurality of detectors on the chip as part of the integrated circuit, so that the detectors are dispersed among the operational-circuits on the chip, the detectors being adapted, in response to radiation incident on the chip, to trigger a security measure so as to prevent tampering with the integrated circuit; and

roughening a surface of the chip so as to defocus radiation incident on the roughened surface.

Claim 101 (canceled)

Claim 102 (canceled)

Claim 103 (currently amended): Circuitry for protection of an integrated circuit, which integrated circuit includes operational-circuits formed on a chip, the circuitry comprising:

a plurality of protective circuits, integrally formed on the chip as part of the integrated circuit and dispersed among the operational-circuits on the chip, the protective circuits being adapted, in response to radiation incident on the chip, to apply a security measure so as to prevent tampering with the integrated circuit,

wherein the operational-circuits include components having predefined attributes, and wherein the protective circuits have at least one

modified attribute, relative to at least one predefined attribute of at least one of the components, so as to alter the response of the protective circuits to the radiation relative to the response of the components having the predefined attributes, and

wherein the chip has an upper surface and a lower surface, and at least one of the upper surface and the lower surface is roughened so as to defocus radiation incident on the roughened surface.

Claim 104 (new): The circuitry according to claim 103 and wherein at least one of the plurality of protective circuits comprises a radiation detector.

Claim 105 (new): The circuitry according to claim 104 and wherein at least one of the plurality of protective circuits comprises an auxiliary circuit coupled with the radiation detector.

Claim 106 (new): The circuitry according to claim 103 and wherein at least one of the protective circuits serves as one of the components in one of the operational-circuits.

Claim 107 (cancelled)

Claim 108 (new): The circuitry according to claim 103 and wherein the predefined attributes are chosen from at least one of: layout attributes; layout dimensions; manufacturing-process attributes; doping dosage; adding a sub-element of the component; removing the sub-element of the component; and materials type.

Claim 109 (currently amended): A method for protection of an integrated circuit, which integrated circuit includes operational-circuits formed on a chip, the method comprising:

integrally forming a plurality of protective circuits on the chip as part of the integrated circuit, so that the protective circuits are dispersed among the operational-circuits on the chip, the protective circuits being adapted, in response

to radiation incident on the chip, to apply a security measure so as to prevent tampering with the integrated circuit,

wherein the operational-circuits include components having predefined attributes, and wherein the protective circuits have at least one modified attribute, relative to at least one predefined attribute of at least one of the components, so as to alter the response of the protective circuits to the radiation relative to the response of the components having the predefined attributes, and

wherein the chip has an upper surface and a lower surface, and the method also comprises roughening at least one of the upper surface and the lower surface so as to defocus radiation incident on the roughened surface.

Claim 110 (new): The method according to claim 109 and wherein at least one of the plurality of protective circuits comprises a radiation detector.

Claim 111 (new): The method according to claim 110 and wherein at least one of the plurality of protective circuits comprises an auxiliary circuit coupled with the radiation detector.

Claim 112 (new): The method according to claim 109 and wherein at least one of the protective circuits serves as one of the components in one of the operational-circuits.

Claim 113 (cancelled).

Claim 114 (new): The method according to claim 109 and wherein the predefined attributes are chosen from at least one of: layout attributes; layout dimensions; manufacturing-process attributes; doping dosage; adding a sub-element of the component; removing the sub-element of the component; and materials type.